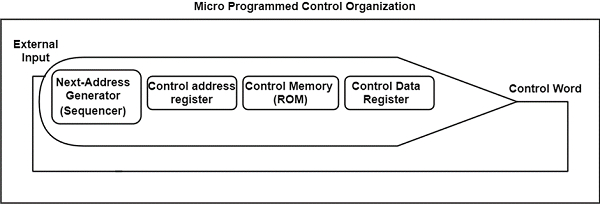
**Micro-programmed Control Unit**

Fig: microprogram sequencer or nest address generator

Symbolic Microinstruction:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Label | Microoperations | CD | BR | AD |
|  |  | U | JMP |  |
|  |  | I | CALL |  |
|  |  | S | RET |  |
|  |  | Z | MAP |  |

Fetch routine:

AR ← PC

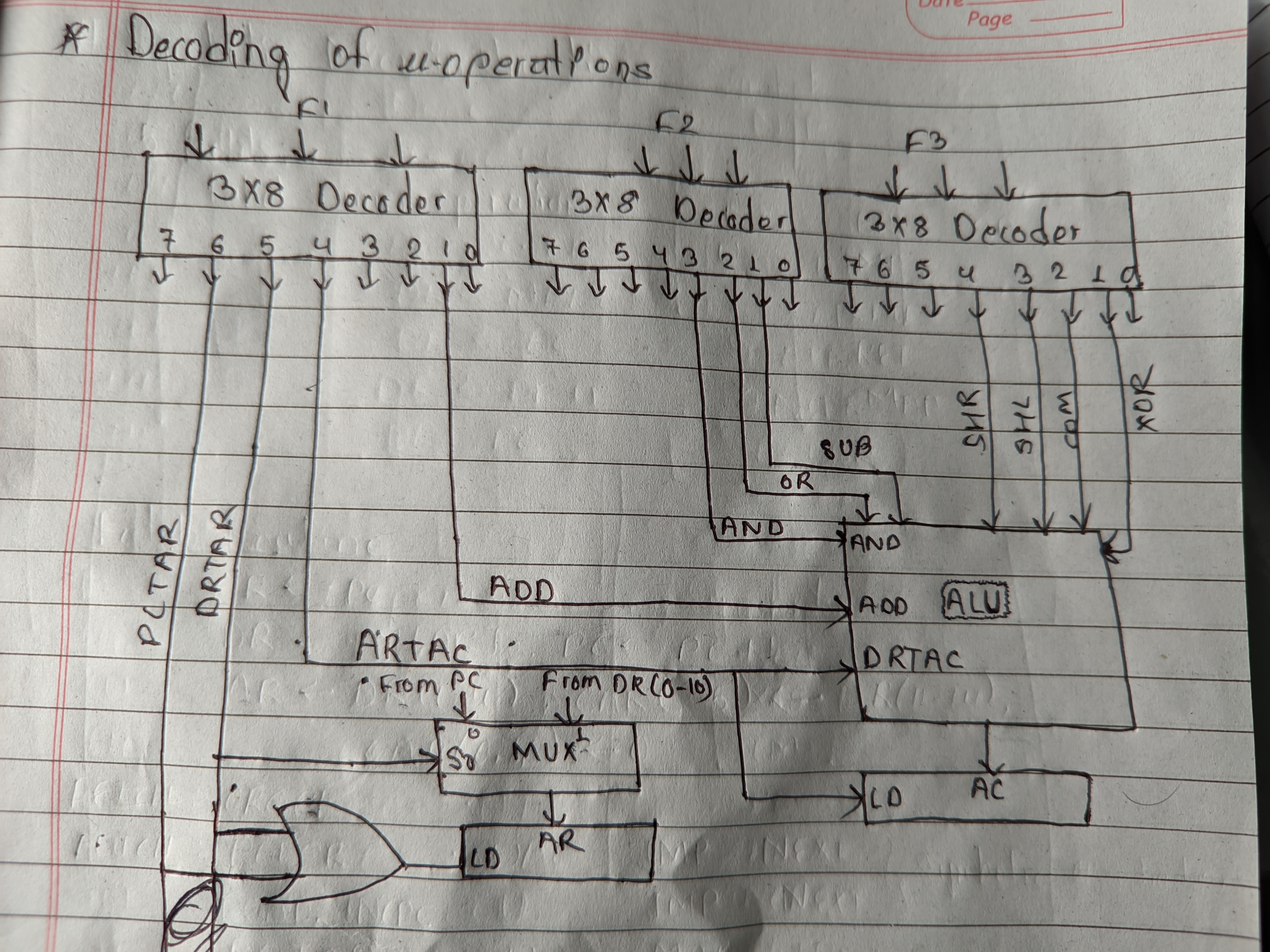
DR ← M[AR] , PC ← PC + 1

AR ← DR(0-10) , CAR(2-5) ← DR(11-14) , CAR(0,1,6) ← 0

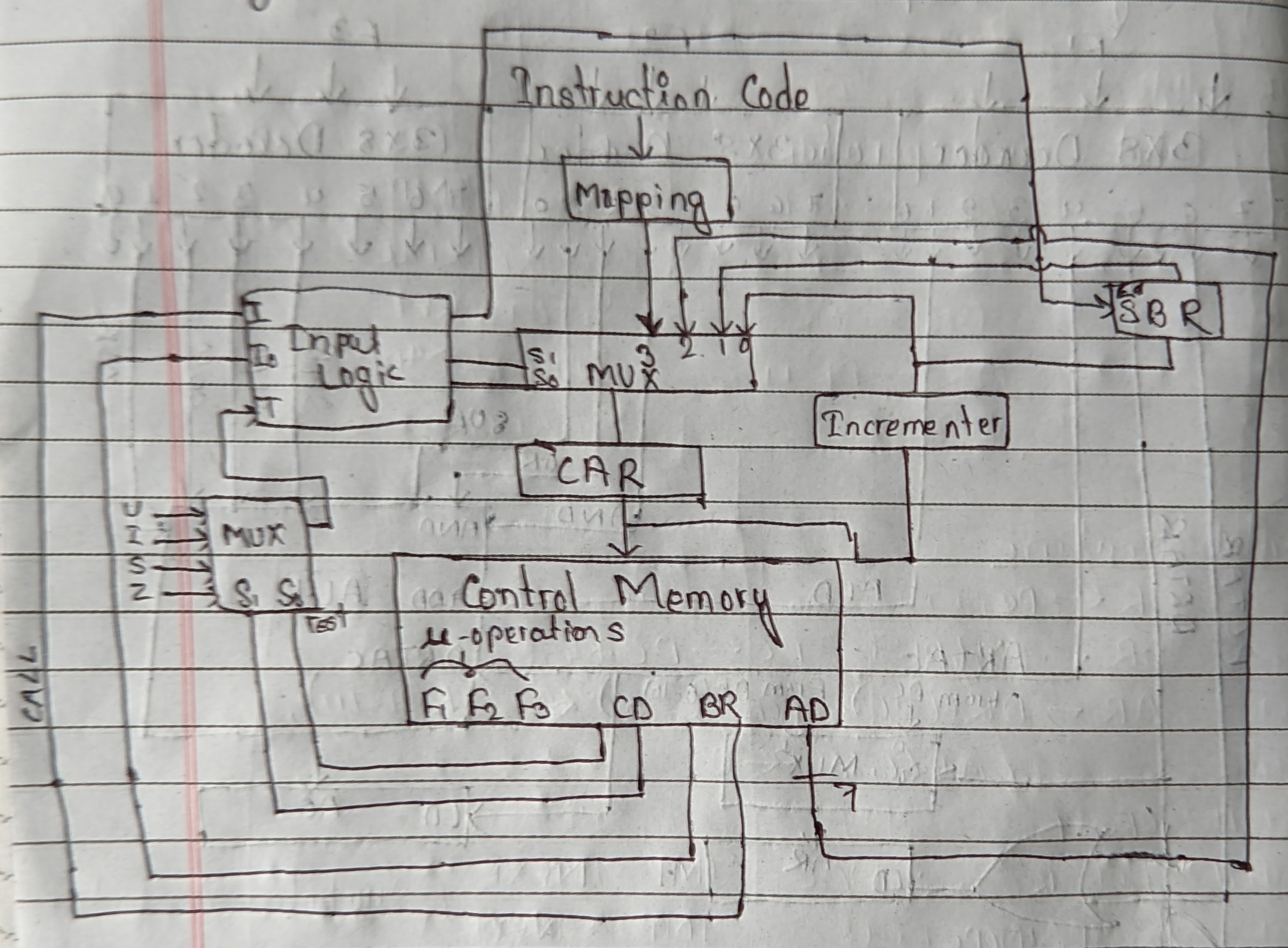
ORG64

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Label | Microoperations | CD | BR | AD |
| FETCH | PCTAR | U | JMP | NEXT |
|  | READ,INCPC | U | JMP | NEXT |
|  | DRTAR | U | MAP |  |
| ABOVE IN BINARY |  |  |  |  |
| 1000000 | 110 000 000 | 00 | 00 | 1000001 |
| 1000001 | 000 100 101 | 00 | 00 | 1000010 |
| 1000010 | 101 000 000 | 00 | 11 | 0000000 |
| Label | Microoperations | CD | BR | AD |
| ADD | NOP | I | CALL | INDRCT |
|  | READ | U | JMP | NEXT |
|  | ADD | U | JMP | FETCH |
|  | ORG 4 |  |  |  |
| BRANCH | NOP | S | JMP | OVER |
|  | NOP | U | JMP | FETCH |
| OVER | NOP | I | CALL | INDRCT |
|  | ARTPC | U | JMP | FETCH |
|  | ORG 8 |  |  |  |
| STORE | NOP | I | CALL | INDRCT |
|  | ACTDR | U | JMP | NEXT |
|  | WRITE | U | JMP | FETCH |

Decoding of microoperations:



Design of control unit:



Circuit for Input logic:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| I1 | I2 | T | S1 | S2 | LOAD SBR |
| 0 | 0 | 0 | 0 | 0 | 0 NEXT |
| 0 | 0 | 1 | 0 | 1 | 0 JMP |
| 0 | 1 | 0 | 0 | 0 | 0 NEXT |
| 0 | 1 | 1 | 0 | 1 | 1 CALL |
| 1 | 0 | X | 1 | 0 | 0 RET |
| 1 | 1 | X | 1 | 1 | 0 MAP |